Latency-Information Theory: A Novel Latency Theory Revealed as Time Dual of Information Theory

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ABSTRACT

This paper outlines a space-time duality study started in 2003 and leading to a latency-information theory (LIT) that unifies information theory with a novel latency theory revealed as time-dual. While information theory guides the design of communication systems, latency theory does the same for recognition systems. A unified recognition-communication system is an intelligence system and LIT illuminates its design. LIT naturally arose from the author's desire to systematically address the design of a real-world intelligence system for DARPA's knowledge-aided sensor signal processing expert reasoning (KASSPER) program. This work has led to practical intelligence system solutions that yield outstanding target detections under severely taxing environments, while also exhibiting several orders of magnitude savings in prior-knowledge storage-space, processing-time, and implementation complexity over standard schemes. Moreover, it has led to the discovery of a mathematical-physical duality guiding life system designs.

***Index Terms*—**Duality, Space, Time, Information, Latency, Intelligence, Life, Mathematics, Physics, Radar

1. INTRODUCTION

Latency-information theory (LIT) is a novel system design methodology that unifies information theory with latency theory, its revealed time-dual. While information theory guides the design of communication systems with noisy channels, latency theory does the same for recognition systems with processing-time limited sensors (PTLSs). A recognition and communication integrated system is an intelligence system and LIT illuminates its design. Starting in 2003 LIT was progressively conceptualized by the author [1] to address the undesirable SINR radar performance of DARPA's knowledge-aided sensor signal processing expert reasoning (KASSPER) program [2] when its intelligence system (a clutter covariance processor (CCP)) processed clutter prior-knowledge in the form of SAR imagery, that had been significantly compressed by a highly lossy and radar independent (or blind) source-coder [3]. This unsatisfactory result was traced to the significant mismatch of the intelligence system to the highly lossy SAR imagery input. LIT addressed this problem by replacing the 'lossless' CCP with a novel 'lossy' processor-coder, the time-dual of a lossy source-coder that is significantly better matched to the lossy SAR imagery. This new kind of lossy intelligence system was found to yield outstanding SINR radar performance under severely taxing environmental disturbances, e.g. antenna array misalignments, channel mismatch, etc. [3], while also exhibiting several orders of magnitude savings in intelligence storage-space, processing-time, and implementation complexity over lossless schemes.

In Section 2 information theory is reviewed. In Section 3 latency theory is presented. In Section 4 LIT is introduced. In Section 5 LIT is applied to knowledge-aided radar. In Section 6 four LIT revelations are highlighted, inclusive of a mathematical-physical duality guiding life system designs.

2. INFORMATION THEORY

In Fig. 1a a communication system is shown consisting of three major parts, plus a twofold channel. These parts are:

1) A source-encoder that extracts the information from a signal-source's intelligence sourced-space (or intel-space, e.g. a 4 Mbytes SAR image), and a source-decoder whose output **X'** reconstructs the signal-source discrete random variable output $\mathbf{X} \in \{a_1,..,a_U\}$. The source-coder is lossless when **X'=X** and lossy otherwise. The source-entropy $\mathcal{H}$ in bits/**X** is the expected source-information guiding as 'lower' performance-bound a lossless source-coder design:

$$\mathcal{H} = \sum_{i=1}^{U} P_S[a_i] I_S(a_i) = \sum_{i=1}^{U} P_S[a_i] \log_2(1/P_S[a_i]) \quad (1)$$

where $I_S(a_i)$ is the source-information in the outcome a_i in bits and $P_S[a_i]$ is the source-probability of obtaining a_i with the 'passing of time'. Thus a lossless source-encoder has a rate $R_{SE}=R_{SE}^{Lossless}$ satisfying $\mathcal{H} \le R_{SE}^{Lossless} \le R_S$ where R_S is the signal-source rate. It is also ideal when $R_{SE}^{Lossless}=\mathcal{H}$. Examples of lossless source-coders are Entropy, Huffman, and Arithmetic coders [4]. Alternatively, a lossy source-coder has a rate $R_{SE}=R_{SE}^{Lossy}$ satisfying $0 \le R_{SE}^{Lossy} < \mathcal{H}$. Examples of lossy source-coders are wavelet, predictive, transform, and predictive-transform (PT) [4]-[6].

2) A channel-encoder after the source-encoder and a channel-decoder before the source-decoder. The channel-encoder advances overhead-knowledge, e.g. parity bits, for the accurate communication of a source-encoder's output through a noisy 'intel-space channel'. The union of a source coder and channel coder is referred here as a channel and

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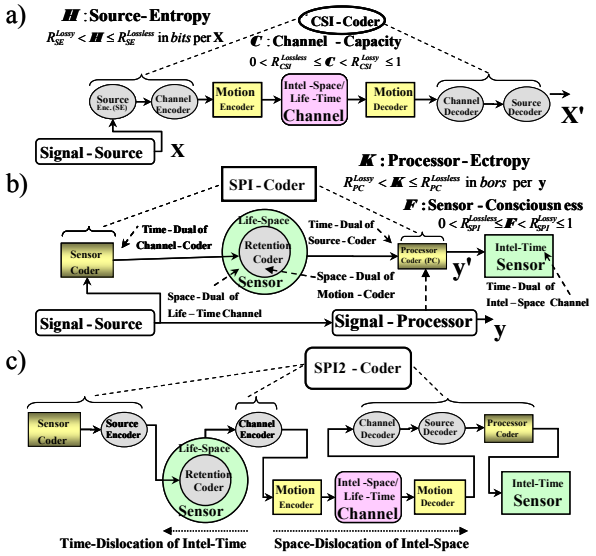

Fig. 1. a) Communication System. b) Recognition System. c) Recognition-Communication (or Intelligence) System

source integrated (CSI) coder where channel appears before source in this designation to emphasize the unique enabling role of a channel-coder in accurate communications.

The CSI-coder design is guided by information-theory's channel-coding [7], also known as 'the mathematical theory of communication'. Channel-coding guides the design of a lossless CSI-coder via a channel-capacity $\mathbf{C}$ 'upper' performance-bound. This bound is defined here as the maximum achievable CSI coder ratio R_{CSI}. R_{CSI} is the ratio of communicated R_{SE}, R_{SE}^{com}(= k bits/X), to space-dislocated channel-encoder rate R_{CE} (= n bits/X), i.e.,

$$0 \le R_{CSI} = R_{SE}^{com} / R_{CE} = k/n \le 1 \qquad (2)$$

where R_{SE}^{com} is smaller than R_{CE}. R_{CSI} is achievable when R_{SE}^{com} is reconstructed by the channel-decoder with an arbitrarily small probability of error. For a memoryless noisy channel with an input $\mathfrak{E}$ and output $\mathfrak{F}$ denoting n-bits random codewords, $\mathbf{C}$ is defined [7] by

$$0 \le \mathbf{C} = (\mathbf{H}_{\mathbf{E}} - \mathbf{H}_{\mathbf{E/F}})/\mathbf{H}_{\mathbf{E}} = \max\{(\mathbf{H}_{\mathfrak{E}} - \mathbf{H}_{\mathfrak{E}/\mathfrak{F}})/\mathbf{H}_{\mathfrak{E}}\} \le 1 \qquad (3)$$

where **E** and **F** are the $\mathfrak{E}$ and $\mathfrak{F}$ cases with a probability distribution $\{P[e_i]\}$ for **E** that maximizes (e.g. a uniform distribution for a binary symmetric channel [7]) the mutual source-information ratio $(\mathbf{H}_{\mathfrak{E}} - \mathbf{H}_{\mathfrak{E}/\mathfrak{F}})/\mathbf{H}_{\mathfrak{E}}$ where $\mathbf{H}_{\mathfrak{E}/\mathfrak{F}}$ is noted to be a *channel-induced intel-space penalty*. A lossless CSI-coder has an achievable $R_{CSI}=R_{CSI}^{Lossless}$ with $0 \le R_{CSI}^{Lossless} \le \mathbf{C}$ and is ideal when $R_{CSI}^{Lossless}=\mathbf{C}$. A lossy CSI-coder has a no achievable $R_{CSI}=R_{CSI}^{Lossy}$ with $\mathbf{C} < R_{CSI}^{Lossy} \le 1$.

3) A motion-coder whose encoder follows the channel-encoder and decoder precedes the channel decoder. This coder enables the space dislocation of intel-space while suffering a *channel-induced life motion-time (or life-time) penalty* which is unavoidable, even without channel interferences, due to the *speed of light* limit in a *vacuum* of c = 2.9979 x 10^8 m/sec. A motion-coder is also referred as a channel and mover integrated (CMI) coder due to its integration of a 'life-time channel' coder, e.g. a mixer or network router addressing a communication channel-induced life-time penalty, and a mover coder, e.g. an antenna system.

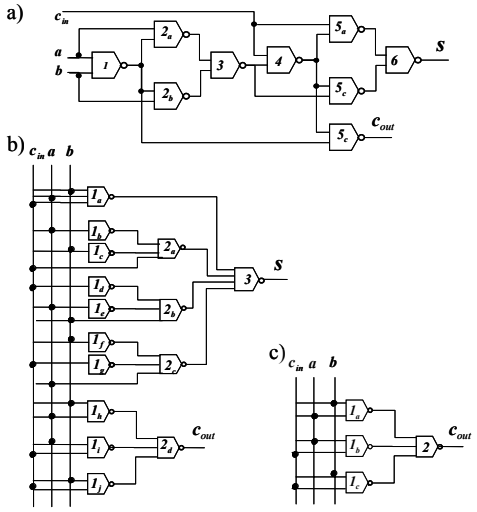

Fig. 2. Full Adder. a) Original Signal-Processor. b) Lossless Processor-Coder. c) Lossy Processor-Coder.

3. LATENCY THEORY

In Fig. 1b a recognition system is shown consisting of three major parts, plus a split twofold sensor. These parts are:

1) A processor-coder that extracts the latency from a signal-processor's intelligence processing-time (or intel-time) in binary operator (bor) units, and whose vector output **y**' reconstructs the signal-processor's vector output **y**. The processor-coder is said to be lossless when **y**'=**y** and lossy otherwise. Three full adder architectures are shown in Fig. 2. First Fig. 2a presents an original full adder (or signal-processor) where its two-input NAND gates perform binary operations. Its input is the vector $\mathbf{x}=[a,b,c_{in}]^t$ where a, b and c_{in} are added bits with c_{in} the carry-in, while its output is the vector $\mathbf{y}=[c_{out},s]^t$ where s and c_{out} are sum and carry-out bits, respectively. The intel-time of the full-adder is then expressed as 6 NAND bors for s and 5 NAND bors for c_{out}. More globally, this same full-adder is characterized by a signal-processor rate R_P in bors/**y** given by the maximum of the intel-times for s and c_{out}, thus R_P = 6 bors/**y**. In Fig. 2b a faster lossless processor-coder is depicted whose intel-time is of 3 bors for s and 2 bors for c_{out} where, for simplicity, it is assumed that the time delay of 4, 3 and 2-input NAND gates is the same. In turn, this processor is characterized by the lossless processor-coder rate $R_{PC}^{Lossless}$ given by the maximum of the intel-times for s and c_{out}, thus $R_{SE}^{Lossless}$=3 bors/(**y'=y**). In Fig. 2c an even faster and also much simpler lossy processor-coder is depicted that only implements the carry-out of the lossless processor-coder of Fig. 2b, thus $\mathbf{y'}=[c_{out},0]^t \ne \mathbf{y}=[c_{out},s]^t$ except when s=0. In particular, this lossy processor has a rate R_{PC}^{Lossy}=2 bors/($\mathbf{y'} \ne \mathbf{y}$).

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Next the processor-ectropy $\mathcal{K}$ in bors/**y**—the time dual of $\mathcal{H}$—is the minmax processor-latency guiding as 'lower' performance-bound a lossless processor-coder design:

$$\mathcal{K} = \max\,(L_P(y_1),..,L_P(y_Z)),\ L_P(y_i) = f_i(C_P[y_i])\ \ i=1,..,z \qquad (4)$$

where $L_P(y_i)$ is y_i's processor-latency in bors with y_i being an element of a signal-processor vector output $\mathbf{y}=[y_1,..,y_z]^t$, $C_P[y_i]$ is the processor-constraint of y_i which depends on 'configuration of space' limitations, and $f_i(.)$ is a function mapping $C_P[y_i]$ to $L_P(y_i)$. As illustration consider Fig. 2a where implementation (or configuration of space) constraints allow us to redesign this full-adder with NAND gates having any number of inputs. Fig. 2b illustrates such a redesign from which the desired latencies of (4) are found, thus $L_P(s) = 3$ bors, $L_P(c_{out}) = 2$ bors and $\mathcal{K} = 3$ bors/**y**. Thus a lossless processor-coder has a $R_{PC} = R_{PC}^{\ Lossless}$ that satisfies the condition $\mathcal{K} \le R_{PC}^{\ Lossless} \le R_P$ and is ideal when $R_{PC}^{\ Lossless}=\mathcal{K}$. A lossy processor-coder, on the other hand, satisfies the condition $0 \le R_{PC}^{\ Lossy} < \mathcal{K}$.

2) A sensor-coder placed prior to a processor-coder. The task of a sensor-coder is to find the prior-knowledge needed to time dislocate (or shift back in time) the onset of the processor-coder's intel-time such that its output can be recognized by a PTLS. This *intel-time* PTLS is the time-dual of a noisy *intel-space* channel. A PTLS condition exists when $\mathcal{K} > R_{PC}^{\ rec} = W$ bors/**y** where $R_{PC}^{\ rec}$ is the part of an ideal processor-coder's $\mathcal{K}$ that is recognized by a sensor whose maximum waiting-time is W in bor units. A simple illustrative example of this condition is when a sequential adder uses the full-adder of Fig. 2a to add two bytes subject to W=12-bors/**y**. Previously it was found that the full adder has the processor-latencies $L_P(s) = 3$ bors and $L_P(c_{out}) = 2$ bors associated with its two outputs. In turn this implies that the processor-ectropy for the sequential 1-Byte adder is of approximately $\mathcal{K}$=2x8=16 bors/**y**. Thus the PTLS condition $\mathcal{K}$=*16 bors*/**y** > $R_{PC}^{\ rec}$ =W=*12 bors*/**y** is satisfied and prior-knowledge must be used. The ratio of $R_{PC}^{\ rec}$ to $\mathcal{K}$ is called the sensor-consciousness $\mathcal{F}$ thus

$$0 \le \mathcal{F} = R_{PC}^{\ rec}/\mathcal{K} \le 1, \qquad (5)$$

where $\mathcal{F}$ is the time-dual of the channel-capacity $\mathcal{C}$ (3). For our example $\mathcal{F}$ = 12/16 = 0.75. Due to the PTLS condition $\mathcal{K} > R_{PC}^{\ rec}$ a recognition-system must time-dislocate the ideal processor-coder's intel-time to an earlier starting-time t_i by the use of prior-knowledge about the processor-coder's input**.** For our running example the necessary time-dislocation is of $\mathcal{K}$-$R_{PC}^{\ rec}$=16-12= 4 bors/**y**. For instance, these four bors of time-dislocation can be accurately achieved if the sensor-coder determines that the two least significant bits of each added byte can be set to zero with a negligible impact on the accuracy of the overall sum (it is assumed that all the byte's bits become simultaneously available). Thus it has been found that an optimum recognition-problem is about finding prior-knowledge to advance the unset of the ideal processor-coder's intel-time for its accurate recognition by a PTLS. The cascade of a sensor-coder and a processor-coder is herein called a sensor and processor integrated (SPI) coder where sensor appears before processor in this designation to emphasize the unique enabling role of a sensor-coder in accurate recognitions.

The $\mathcal{F}$ definition can also be stated as the time-dual of that for $\mathcal{C}$ (3). $\mathcal{F}$ is then the maximum achievable SPI-coder ratio R_{SPI} where R_{SPI} is given by the ratio of $R_{PC}^{\ rec}$ to the sensor-coder rate R_{SC}. R_{SC} is equal to $R_{PC}^{\ rec}$ plus the amount of time-dislocation that the sensor-coder must provide, i.e., R_{PC} - $R_{PC}^{\ rec}$, for the full recognition of R_{PC} by the PTLS. Thus $R_{SC} = R_{PC}^{\ rec} + R_{PC} - R_{PC}^{\ rec} = R_{PC}$ where R_{PC} is equal to T, the intel-time of the processor-coder in bors per **y** and

$$0 \le R_{SPI} = R_{PC}^{\ rec}/R_{SC} = W/T \le 1. \qquad (6)$$

R_{SPI} is achievable when the processor-coder is both lossless and has an output arbitrarily close to the signal-processor's output (MSE can be used as a measure). For a PTLS with an n-dimensional input $\mathbf{y}(t_i+T)$ and output $\mathbf{z}(t_i+W)=\mathbf{y}(t_i+W)$ $\mathcal{F}$ is

$$0 \le \mathcal{F} = (\mathcal{K}_{\mathbf{y}} - \mathcal{K}_{\mathbf{y/z}})/\mathcal{K}_{\mathbf{y}} = \max\{(\mathcal{K}_{\mathbf{y}} - \mathcal{K}_{\mathbf{y/z}})/\mathcal{K}_{\mathbf{y}}\} \le 1 \qquad (7)$$

where **y** and **z** denote the $\mathbf{y}$ and $\mathbf{z}$ cases associated with constraints $\{C[y_i]\}$ for **y** that maximizes the mutual processor-latency ratio $(\mathcal{K}_{\mathbf{y}} - \mathcal{K}_{\mathbf{y/z}})/\mathcal{K}_{\mathbf{y}}$ where $\mathcal{K}_{\mathbf{y/z}}$ is noted to be a *sensor-induced intel-time penalty*. For instance, for our 1-byte adder example the best $\{C[y_i]\}$ allows NAND gates with an arbitrary number of inputs, leading to $\mathcal{K}_{\mathbf{y}}$=16 bors, $\mathcal{K}_{\mathbf{y/z}}$=4 bors since W=12 bors, and $\mathcal{F}$=*0.75*. Similarly to $\mathcal{C}$, $\mathcal{F}$ is an 'upper' performance-bound that guides the design of lossless SPI-coders. A lossless SPI-coder has an achievable $R_{SPI}=R_{SPI}^{\ Lossless}$ with $0 \le R_{SPI}^{\ Lossless} \le \mathcal{F}$ and is ideal when $R_{SPI}^{\ Lossless}=\mathcal{F}$. A lossy SPI-coder has a no achievable $R_{SPI}=R_{SPI}^{\ Lossy}$ with $\mathcal{F} < R_{SPI}^{\ Lossy} \le 1$. The previously described sensor-consciousness viewpoint is named sensor-coding and guides the design of recognition-systems. Sensor-coding is also called 'the mathematical theory of recognition' just like channel-coding is for the communication case [7].

3) A retention-coder placed after the sensor-coder. This coder is a storage device that enables the time dislocation of intel-time while suffering a *sensor-induced life retention-space (or life-space) penalty* which is unavoidable, even without sensor interferences, due to the *pace of dark* limit in a black-hole of $\mathcal{X}=960\pi c^2/hG$ = 6.1123 x 10^{63} sec/m^3, first advanced in [1] as the space-dual of the speed of light, where h is Plank's constant and G is the gravitational constant. A retention-coder is also referred as a sensor and retainer integrated (SRI) coder due to its integration of a 'life-space sensor' coder, e.g. a surface mounted leadless chip carrier that addresses a recognition sensor-induced life-space penalty, and a retainer coder, e.g. a silicon semiconductor.

4. LATENCY-INFORMATION THEORY

In Fig. 1c a recognition-communication (or intelligence) system is shown. A source-encoder is placed after the sensor-coder to reduce the stored retention-coder intel-space, while the source-decoder is placed prior to the processor-coder. On the other hand, the channel-encoder is

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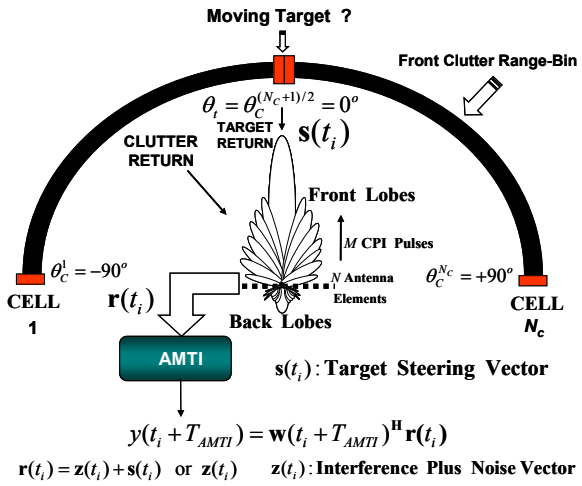

Fig. 3. Airborne Radar System

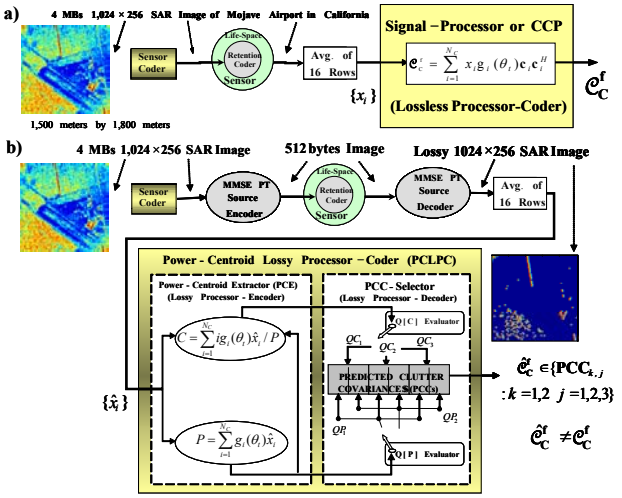

Fig. 4. a) SPI (or SPI0) Coder Intelligence System. b) SPI1-Coder Intelligence System.

located after the retention-coder for the accurate communication of the retention-coder intel-space, while the channel-decoder is placed before the source-decoder. The motion-encoder is positioned after the channel-encoder to space dislocate the channel-encoder intel-space. The intelligence system of Fig. 1c can then be used to define three types of SPI-based intelligence coders. These intelligence coders are: 1) the bare bones SPI0-coder (or SPI-coder) of Fig. 1b, lacking a communication system; 2) a more capable (or wiser) SPI1 coder, using a source-coder to reduce the stored retention-coder intel-space; and 3) the most capable (or wisest) SPI2-coder of Fig. 1c, using the entire communication system to both reduce the stored retention-coder intel-space and to accurately communicate the retention-coder intel-space through a noisy channel .

The design of the SPI2 intelligence coder, with SPI0 and SPI1 coders as special cases, is guided by sensor-channel coding which unifies channel-coding and sensor-coding. Sensor-channel coding is the same as 'the mathematical theory of intelligence'.

5. KNOWLEDGE-AIDED RADAR

Next a SPI1 intelligence coder is advanced for the knowledge-aided radar system of Fig.3. This figure presents three basic structures. First a front clutter range-bin is seen where it is of interest to determine if a moving target exists with a bore-sight angle θ_t of zero degrees, i.e. $\theta_t = 0^0$. The range-bin is also noted to be decomposed into an even number of cells N_C where the boundary line between cells $N_C/2$ and $(N_C+2)/2$ is investigated to determine if a moving target appears there. Second an N elements antenna array is presented which radiates M pulses during a CPI where the antenna pattern points towards the assumed target location. Third an airborne moving target indicator (AMTI) is shown. The AMTI receives its input from the antenna receiver, inclusive of clutter range-bin returns as well as other kinds of radar system disturbances. This input is modeled at the time instant t_i by the NM-dimensional complex vector $\mathbf{r}(t_i)=\mathbf{z}(t_i)+\mathbf{s}(t_i)$ where $\mathbf{s}$ is the steering vector of the assumed target and $\mathbf{z}$ contains undesirable signals, inclusive of clutter, jammer, range walk, internal clutter motion, channel mismatch, antenna white noise, and antenna array misalignment [3]. The output of the AMTI at the later time instant t_i+T_{AMTI} is the complex scalar signal $y(t_i+T_{AMTI})$ with T_{AMTI} denoting the AMTI processing delay. In turn, the relationship between the ATMI input and output is given by

$$y(t_i+T_{AMTI}) = \mathbf{w}(t_i+T_{AMTI})^H \mathbf{r}(t_i), \quad \mathbf{w}(t_i+T_{AMTI}) = \mathrm{C}^{-1}\mathbf{s}(t_i) \quad (8)$$

$$\mathrm{C}=\{(\mathcal{C}_c^f + \mathcal{C}_c^b)\mathrm{O}(\mathrm{C}_{RW} + \mathrm{C}_{ICM} + \mathrm{C}_{CM})\} + \mathrm{C}_J \mathrm{O} \mathrm{C}_{CM} + \mathrm{C}_n \quad (9)$$

where: a) C is the NM x NM covariance matrix of $\mathbf{z}$, i.e. $\mathrm{C} = \mathrm{E}[\mathbf{z}\mathbf{z}^H]$; b) $\mathbf{C}_n$, $\mathcal{C}_c^f$, $\mathcal{C}_c^b$, $\mathbf{C}_J$, $\mathbf{C}_{RW}$, $\mathbf{C}_{ICM}$ and $\mathbf{C}_{CM}$ are NM x NM covariance matrices with the assignment of $\mathbf{C}_n$ to thermal white noise, $\mathcal{C}_c^f$ to front clutter, $\mathcal{C}_c^b$ to back clutter, $\mathbf{C}_J$ to jammer; $\mathbf{C}_{RW}$ to range walk; $\mathbf{C}_{ICM}$ to internal clutter motion; and $\mathbf{C}_{CM}$ to channel mismatch (CM); c) the symbol 'O' denotes a Hadamard product or element by element multiplication: and d) $\mathbf{w}(t_i+T_{AMTI})$ is an NM x 1 complex weighing vector available at the time instant t_i+T_{AMTI}. The relationships (8)-(9) result from maximizing the signal to interference plus noise ratio (SINR) expression

$$\mathrm{SINR}=\mathbf{w}^H\mathbf{s}\mathbf{s}^H\mathbf{w}/\ \mathbf{w}^H\mathrm{C}\mathbf{w} \quad (10)$$

with respect to the weight vector $\mathbf{w}$ where $\mathbf{w}^H\mathbf{s}\mathbf{s}^H\mathbf{w}$ is the power of the target (or signal) return $\mathbf{s}$ and $\mathbf{w}^H\mathrm{C}\mathbf{w}$ is the power of the interference plus noise $\mathbf{z}$. Of all the covariances in (9) only the front clutter covariance $\mathcal{C}_c^f$ is assumed unknown and determined on-line by the signal-processor depicted in the SPI0-coder of Fig. 4a. The signal-processor or CCP evaluates the expression

$$\mathcal{C}_c^f = \sum_{i=1}^{N_C} x_i g_i(\theta_t)\mathbf{c}_i\mathbf{c}_i^H \quad (11)$$

where: 1) $\{x_i: i=1,..N_C\}$ are N_C scalar resolution clutter cell power in dBs available from a SAR image range-bin with N_C=256 assumed. More specifically, $\{x_i: i=1,..256\}$ is found

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by averaging 16 rows of a 4 Mbytes (MBs) 1024x256 SAR image of the Mojave Airport in California that is extracted from the retention-coder; 2) $\{g_i(\theta_t)$:i=1,..,$N_C\}$ are N_C antenna scalar gains with their values found from

$$g_i(\theta_t) = K^f \left| \sin\left\{ N\pi \frac{d}{\lambda}(\sin(\theta_C^i) - \sin(\theta_t)) \right\} / \sin\left\{ \pi \frac{d}{\lambda}(\sin(\theta_C^i) - \sin(\theta_t)) \right\} \right|^2 \quad (12)$$

where θ_C^i is the i^{th} clutter cell bore-sight angle, θ_t is the target bore-sight angle, d is the antenna inter-element spacing, λ is the operating-wavelength, and K^f is the front antenna gain constant. 3) $\{\mathbf{c}_i\mathbf{c}_i^H$:i=1,..$N_C\}$ are N_C NMxNM $\mathbf{c}_i\mathbf{c}_i^H$ complex matrices where $\mathbf{c}_i$ is the steering vector of the i^{th} clutter cell which is also a function of θ_{AAM} the antenna array misalignment angle (details in (2.17) of [3]). It is assumed that N=16 and M=16 thus $\mathbf{c}_i\mathbf{c}_i^H$ is 256x256 for all i.

The CCP processor-ectropy $\mathcal{K}$ is next found using three constraints. They are: 1) the N_C=256 complex matrices $\{x_i g_i \mathbf{c}_i\mathbf{c}_i^H = x_i\mathbf{M}_i\}$ are simultaneously evaluated by 256 sub-processors where it is assumed that $\mathbf{M}_i$ is evaluated off-line; 2) the 2x256^2=131,072 basic multiplications of $x_i\mathbf{M}_i$ are sequentially executed by each sub-processor; and 3) the sum of the 256 matrices $\{x_i\mathbf{M}_i\}$ leading to $\hat{\mathbf{e}}_c^f$ is implemented with 255 matrix additions. Under these constraints the $\mathcal{K}$ exhibited by the ideal lossless processor-coder is given by $\mathcal{K}$=131,072b_M + 255b_A bors/ $\hat{\mathbf{e}}_c^f$ where b_M is the number of bors per sequential multiplication and b_A is the number of bors per matrix addition. When finding the expression for $\mathcal{K}$ it was both assumed that the latency of each complex scalar element of $\hat{\mathbf{e}}_c^f$ is the same and any time-delays introduced by memory read/write operations are reflected in the b_M and b_A values. Moreover, since the number of matrix additions is significantly less than the number of sequential multiplications and it is also assumed that $b_M >> b_A$, $\mathcal{K}$ can be approximated by 131,072b_M bors/ $\hat{\mathbf{e}}_c^f$.

The SPI1-coder that is used to replace the SPI0-coder of Fig. 4a is shown in Fig. 4b. It consists of the cascade of five subsystems. They are: 1) a sensor-coder advancing 4 MBs SAR imagery; 2) a lossy MMSE PT source-encoder compressing SAR imagery by a factor of 8,172=4MB/512B; 3) a retention-coder retaining the compressed SAR imagery: 4) a MMSE PT source-decoder followed by the averaging of 16 lossy SAR image rows leading to $\{\hat{x}_i$:i=1,..$N_C\}$; and 5) a power-centroid lossy procesor-coder (PCLPC). In particular, the PCLPC consists of a power-centroid extractor (PCE) in cascade with a predicted clutter covariance (PCC) selector. The PCE evaluates the power P and centroid C of the $\{g_i(\theta_i)\}$-weighted lossy intelligence $\{\hat{x}_i : i = 1,..,N_C\}$

$$P = \sum_{i=1}^{N_C} g_i(\theta_t)\hat{x}_i, \qquad C = \sum_{i=1}^{N_C} i g_i(\theta_t)\hat{x}_i / P \quad (13)$$

The PCC-selector, on the other hand, quantizes P and C

$$Q[P] = \begin{Bmatrix} QP_2, & QP_1 < P \le QP_2 \\ QP_1, & P_{\min} \le P \le QP_1 \end{Bmatrix}, \quad \begin{matrix} QP_1 = (P_{\min} + P_{\max})/2 \\ QP_2 = P_{\max} \end{matrix} \quad (14)$$

$$Q[C] = \begin{Bmatrix} QC_3, & (QC_2 + QC_3)/2 < C \le N_C \\ QC_2, & (QC_1 + QC_2)/2 < C \le (QC_2 + QC_3)/2 \\ QC_1, & 1 \le C \le (QC_1 + QC_2)/2 \end{Bmatrix}, \quad \begin{matrix} QC_1 = QC_2 - D \\ QC_2 = (N_C + 1)/2 \\ QC_3 = QC_2 + D \end{matrix} \quad (15)$$

where QP_i and QC_i are quantization levels for P and C, respectively. The parameters P_{max}, P_{min}, and D of (14)-(15) are appropriately found from the SAR image. The quantization levels are then used to select from a memory device one of six PCCs. The PCCs are derived *off-line* from

$$\mathbf{PCC}_{k,j} = X_{k,j} \sum_{i=1}^{N_C} g_i(\theta_t = \theta_c^{QC_j})\mathbf{c}_i\mathbf{c}_i^{\mathbf{H}}, \quad X_{k,j} = QP_k / \sum_{i=1}^{N_C} g_i(\theta_t = \theta_c^{QC_j}) \quad (16)$$

From (16) it is noted that $\mathrm{PCC}_{k,j}$ is a function of QP_k and the antenna gains $\{g_i(\theta_t = \theta_C^{QC_j})\}$ where the j=2 case gives the *physically* build antenna pattern of Fig. 3. Finally, the on-line PCLPC processing-time is noted to be governed by the PCE (13) since the PCC-selector processing-time is small.

The evaluation of $\hat{\mathbf{e}}_c^f$ by the PCLPC leads to a R_{PC}^{Lossy} of one b_M bors/ $\hat{\mathbf{e}}_c^f$ where the availability of appropriate parallel-processing computational resources is assumed. Thus an estimated on-line processing-time improvement of $\mathcal{K}/R_{PC}^{Lossy}$=131,072 results from replacing the lossless ideal CCP with the significantly simpler lossy PCLPC.

Next the *SINR* performance of the SPI1-coder of Fig. 4b is contrasted with that of the same SPI1-coder except that its *lossy* PCLPC is replaced with Fig. 4a's *lossless* CCP (11). The results are shown in Fig. 5 which assume the following radar parameters [3]:1) *Antenna, N*=16, M =16, d/λ=½, σ_n^2=1 (white noise variance), K^f = 56 dBs, K^b = -40 dBs (back antenna-gain), $f_c = 10^9$ Hz (carrier freq.), $f_r = 10^3$ Hz (pulse repetition freq.), θ_{AAM}= 2°; 2) *Clutter,* N_c = 256, D=18, P_{min} = 41 dBs, P_{max} = 74 dBs, 41 dBs=P_{min}/σ_n^2< $10\log_{10}$ CNR^f < P_{max}/σ_n^2 =74 dBs (front clutter to noise ratio CNR^f), $10\log_{10}$ CNR^b = -40 dBs (back clutter to noise ratio CNR^b), β =1 (ratio of distance traveled by radar during pulse repetition interval to d/2); 3) *Jammers,* were not used but similar positive results are derived when they are used [3]; 4) *Range walk,* ρ= 0.999999; 5) *ICM*, b = 5.7 (shape-factor), ω=15 mph (wind-factor); 6) *Narrowband CM,* $\Delta\varepsilon_i$=0 for all i (amplitude error), $\Delta\gamma_i$ fluctuates with a 5° rms for all i (phase-error); 7) *Finite-bandwidth CM,* $\Delta\varepsilon$=0.001 (amplitude peak deviation), $\Delta\phi$= 0.1° (phase peak deviation); 8) *Angle-dependent CM,* B=10^8 Hz (bandwidth), $\Delta\theta$ = 28.6° (main beamwidth).

For each range-bin of SAR image SINR versus normalized Doppler is found for several different cases. In Fig. 5a three cases are displayed for range-bin #1. The first case is the optimum SINR of the SPI0 coder of Fig. 4a. The second and third cases use the lossy SAR image of Fig. 4b. An average SINR error (ASE) of 1.04 dBs is derived when using the lossy PCLPC and an ASE = 4.8 dBs when using a lossless CCP. In Fig. 5b the ASE is plotted versus range-bin number for both the lossy PCLPC and lossless CCP with the lossy case outperforming the lossless one by an average ASE of 4.5 dBs. Finally, it is noted, that the SPI2-coder

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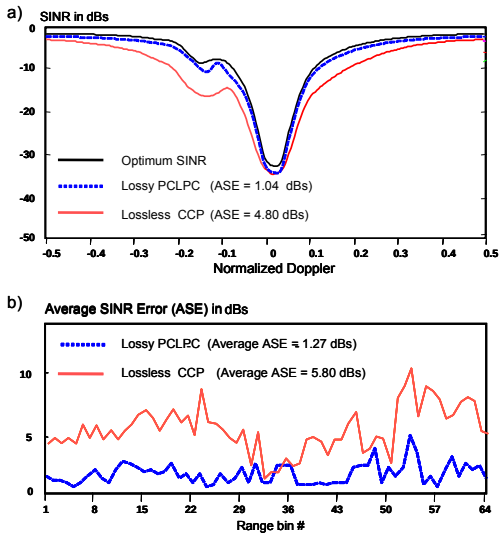

Fig. 5. Lossy PCLPC and Lossless CCP SINR Performance. a) Range-Bin #1 Only. b) All 64 Range-Bins of SAR Image.

of Fig. 1c must be used when the lossy SAR imagery resides in a remote central command station.

6. LIT REVELATIONS

Four LIT revelations are highlighted:

1) The unsatisfactory CCP SINR results of Fig. 5 can be traced to the mismatch between the original SAR image whose covariance the CCP evaluates and the highly lossy SAR image of Fig. 4b that the CCP uses instead in its evaluation. On the other hand, the PCLPC satisfactory SINR results of Fig. 5 can be traced to the significant *lossy SAR image compensation* resulting from some PCCs being designed *off-line* (16) using two *compensating antenna patterns* (CAPs) that do not match the physical one of Fig. 3 pointing to $QC_2=(N_C+1)/2$. Instead, these two CAPs point in the directions of QC_1 and QC_3.

2) Symmetries in the six PCCs of Fig. 4b permit the use of only four PCCs by letting $QC_3 \rightarrow QC_1$ after QC_3 is evaluated, or vice-versa. This low number of PCCs also allows their efficient storage for a suitable number of θ_{AAM} cases.

3) The lossy PCLPC is the time-dual of a lossy transform intel-space coder $\hat{\mathbf{z}} = T_k^t \hat{\mathbf{c}}_k = T_k^t Q(\mathbf{c}_k) = T_k^t Q(T_k \mathbf{z})$ [5] where: $\mathbf{c}_k = T_k \mathbf{z}$ is the encoder with $\mathbf{z}$ a real *nx1* vector input, T_k a real *kxn* matrix with $k<<n$, and $\mathbf{c_k}$ a *kx1* output vector; $\hat{\mathbf{c}}_k = Q(\mathbf{c}_k)$ quantizes $\mathbf{c_k}$; and $\hat{\mathbf{z}} = T_k^t \hat{\mathbf{c}}_k$ is the decoder with lossy output $\hat{\mathbf{z}} \neq \mathbf{z}$. Thus the PCLPC's PCE is an intel-time encoder that is the time dual of $\hat{\mathbf{c}}_k = Q(T_k \mathbf{z})$ and the PCLPC's PCC-selector is an intel-time decoder that is the time dual of $\hat{\mathbf{z}} = T_k^t \hat{\mathbf{c}}_k$. Also, while $\hat{\mathbf{z}} = T_k^t \hat{\mathbf{c}}_k$ is an 'uncertainty' model for a signal-source [5], the PCC-selector is a 'certainty' model for a signal- processor with its output a known PCC.

4) The surfacing of a LIT mathematical (M)-physical (P) duality leading to the unified guidance of intelligence and

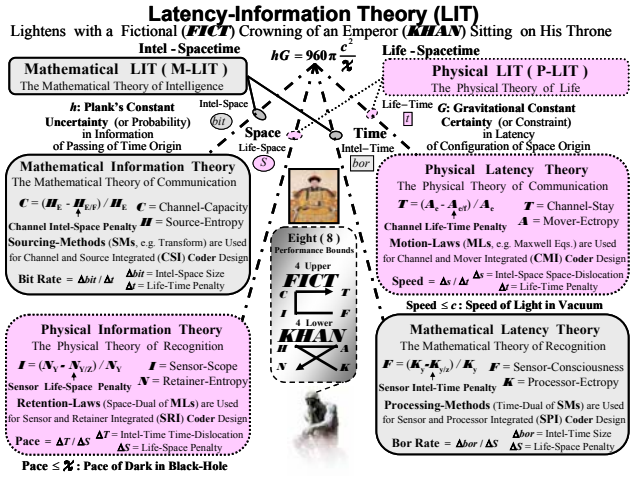

Fig. 6. A Genial Reminder of LIT's Unified Guidance of Intelligence and Life System Designs.

life system designs described in Fig. 6 and [8]. First an intel-spacetime M-LIT integrates M-information and M-latency theories to guide SPI-CSI coder designs via two lower $\boldsymbol{H}$, $\boldsymbol{K}$ and two upper $\boldsymbol{C}$, $\boldsymbol{F}$ performance-bounds. Intel-time processing methods arise as time dual of intel-space sourcing methods, e.g. a lossy PCLPC from a lossy transform source-coder. Secondly a complementary life-spacetime P-LIT integrates P-information and P-latency theories to guide SRI-CMI coder designs via two lower *retainer-entropy* $\boldsymbol{N}$, *mover-ectropy* $\boldsymbol{A}$ and two upper *sensor-scope* $\boldsymbol{I}$, *channel-stay* $\boldsymbol{T}$ performance-bounds. While $\boldsymbol{N}$ is the expected retainer-information in physical space units, $\boldsymbol{A}$ is the minmax mover-latency in physical time units, thus their definitions emulate those of $\boldsymbol{H}$ (1), $\boldsymbol{K}$ (4), respectively [1]. In addition, the $\boldsymbol{I}$, $\boldsymbol{T}$ ratio definitions emulate those for the $\boldsymbol{C}$ (3), $\boldsymbol{F}$ (7) ratios, respectively. Finally, retention (or life-space sourcing) laws surface as space dual of motion (or life-time processing) laws.

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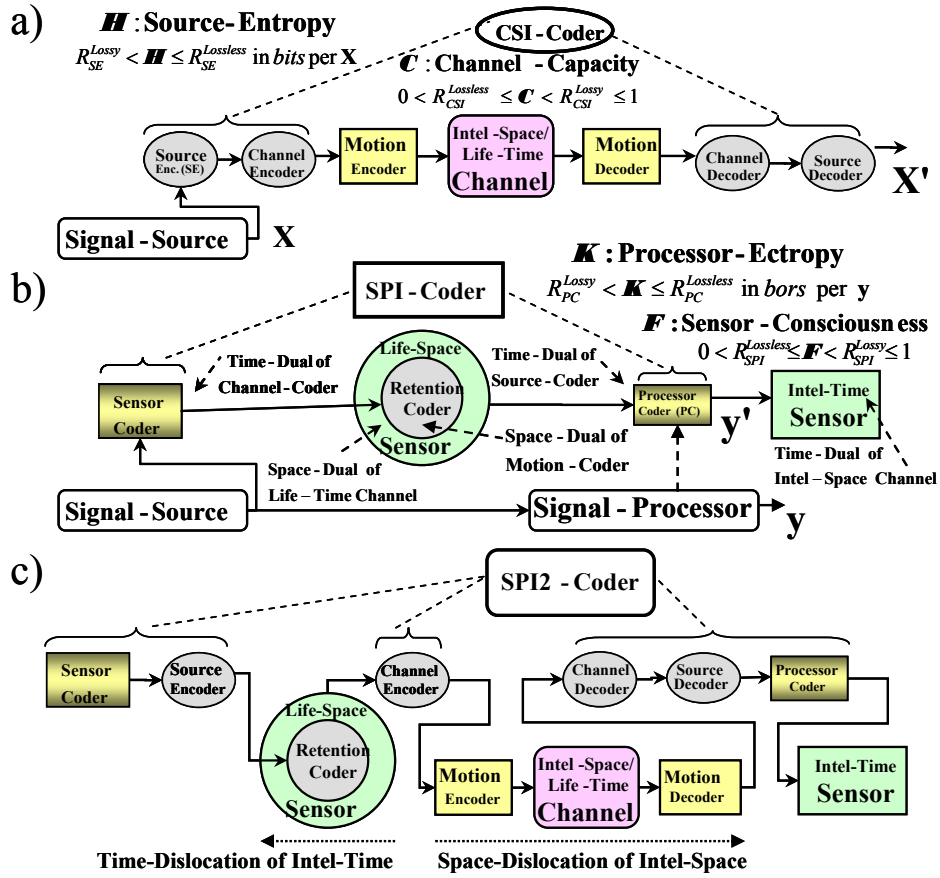

Fig. 1. a) Communication System. b) Recognition System. c) Recognition-Communication (or Intelligence) System

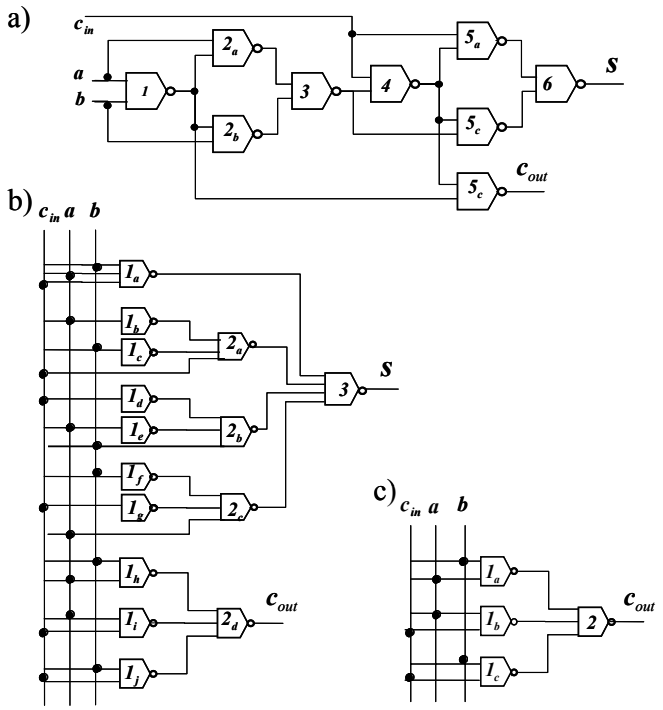

Fig. 2. Full Adder. a) Original Signal-Processor. b) Lossless Processor-Coder. c) Lossy Processor-Coder.

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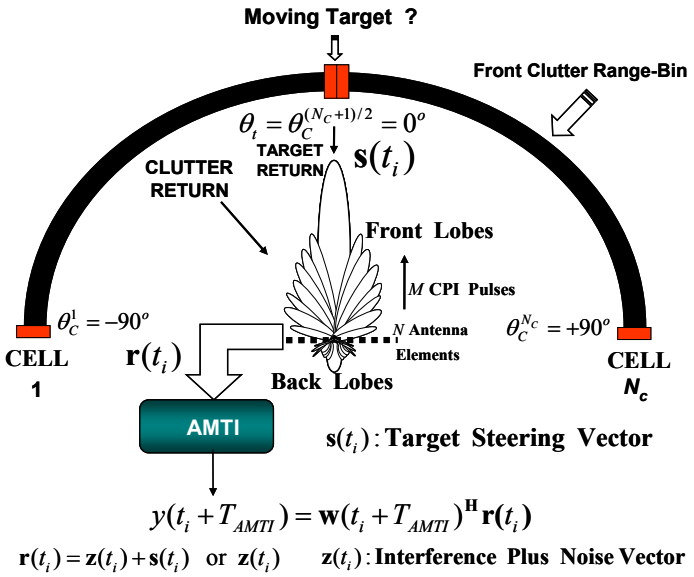

Fig. 3. Airborne Radar System

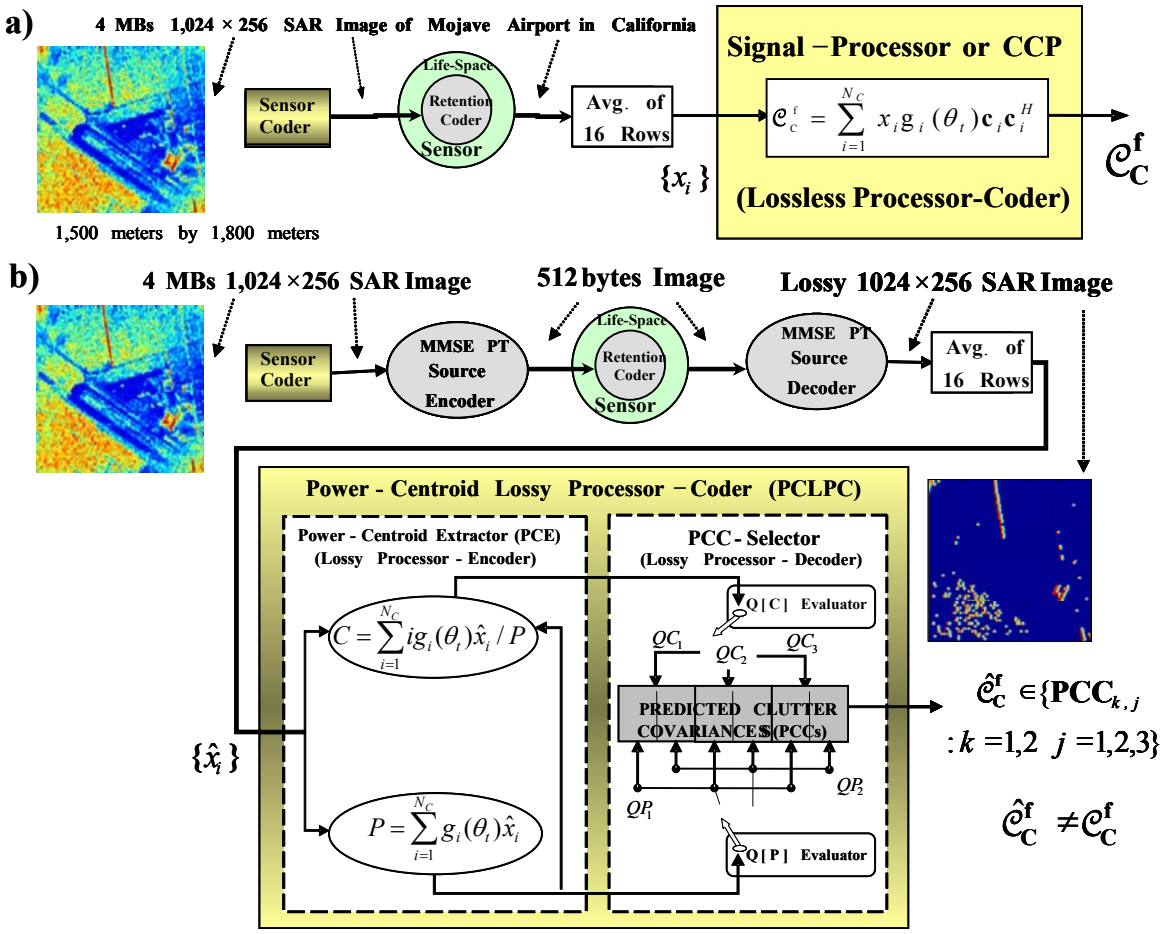

Fig. 4. a) SPI (or SPI0) Coder Intelligence System. b) SPI1-Coder Intelligence System.

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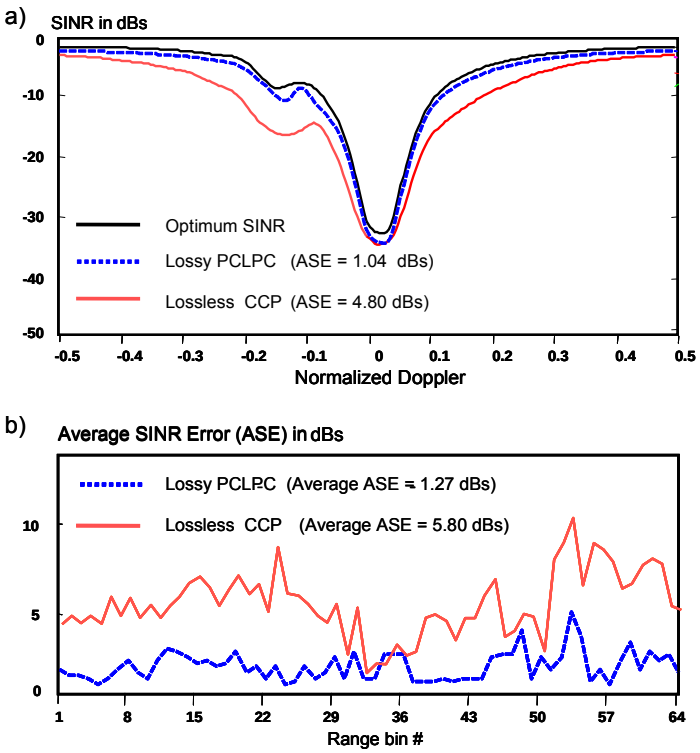

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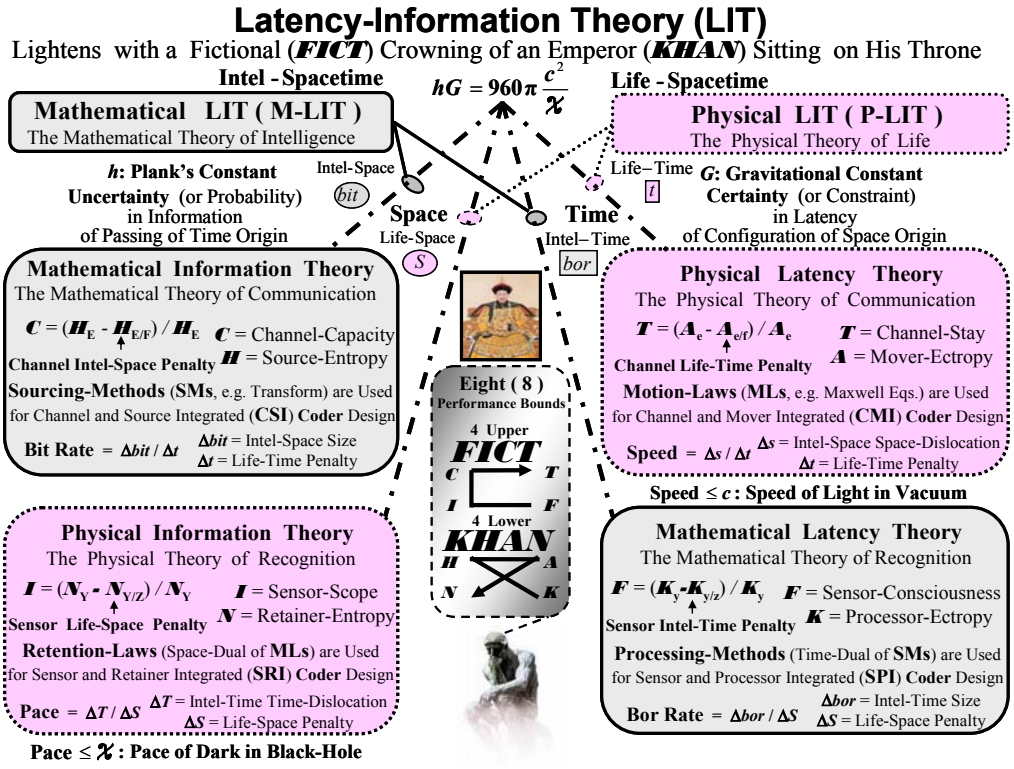

Fig. 6. A Genial Reminder of LIT's Unified Guidance of Intelligence and Life System Designs.

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